

Appl. No. 10/605,428
Andt. dated November 8, 2004
Reply to Office action of August 25, 2004

AMENDMENTS TO THE SPECIFICATION

After paragraph [0028], add new paragraph [0028.1]:

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Fig. 13 is a diagram showing a delay unit being formed by a delay chain of inverters.

In paragraph [0039]:

10 It should also be noted that although throughout the detailed description of the present invention CMOS transistors have been used with n-type first positive and negative side switch elements, it is also possible to use bipolar transistors or p-type first positive and negative switch elements. Additionally, the precharge voltage can be changed to voltages other than VDD. For example, if the first positive and negative side switch
15 elements are implemented with p-type transistors, the precharge switch element should be implemented as an n-type transistor being connected to a precharge voltage such as ground. Furthermore, the purpose of the delay unit ~~it is to~~ is to delay the first control signal SW1 to produce the second control signal SW2. As shown in Fig. 13, it is ~~It is~~ also possible to use other delay units 60 such as a delay chain 300 of inverters 302 and a low
20 pass filter connected to the output of the delay chain 300. For differential implementations, the center switch element is an optional component that lowers the overall switch turn-on resistance and could be omitted while still following the teachings of the present invention.

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